Validating Log-normal Distribution of Delay Variability in Near-Threshold Design

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Abstract: The era of ultra-low power system on chips(SoCs), driven by internet of things(IoTs) and wireless sensor network(WSN), has never seemed this close. While the market is ready for the emergence of these tiny devices, the emergence itself is facing a few obstacles in SoC designs operating in near-threshold region. In this work, we perform an in-depth exploration of delay/slew variability of standard cells operating at near-threshold voltage. Our analysis targets 92 timing arcs in total from 22 cells, each of which include 56 slew/capacitance conditions which are configured in consideration of ultra-low power operation. It turns out that Log-normal probability density function(PDF) model displays a moderately accurate result out of the box, i.e. without further fitting algorithm, although it yields high error in a few slew ranges. In fact, it is discovered that the accuracy of calculated 3 σ/μ varies with different input slew values. While log-normal modeling methodology looks promising, a better fitting methodology or perhaps an alternative modeling technique may be required to overcome its inconsistency over a variation of cap./slew conditions in order to adapt to commercial EDA flow.

Keywords—**Near-Threshold, Log-normal Distribution, Cell Characterization, Delay Modeling**

1. Introduction

SoC designers in the era of ultra-low power design is most likely to suffer from a very strict power/area constraints. It is thus of a high importance that we enable an accurate timing analysis which will lead us to a more optimized circuits. Unfortunately, the accuracy of timing analysis in near-threshold design severely suffers from on-chip parametric variations. The first step towards variability-aware timing analysis is thus an accurate variability modeling method to enable statistical static timing analysis(SSTA).

It is widely known that that under process variations, the Probability Density Function(PDF) of slew/delay is non-Gaussian in near- or sub-threshold region. One promising approximation of the delay/slew variability from literature is log-normal distribution [1][3][6], yet no in-depth exploration has been performed to compare the accuracy of the model in different output capacitance and input slew configurations.

In this work, we initiate an exploration on the accuracy of the log-normal estimation through various output capacitance/input slew conditions. Our analysis targets 92 timing arcs in total from 22 cells, each of which include 56 slew/capacitance conditions which are configured in consideration of ultra-low power operation. Log-normal distribution model displays a moderately accurate result out of the box, i.e. without further fitting algorithm, although it yields high error in some slew range. These characteristics are shared across most cells. We show that the log-normal approximation is still promising, by comparing 3 σ/μ error with $3\sigma + \mu$ error, latter of which is the actual result of delay model and yields an acceptable delay/slew error compared to the those from literature.

2. Related Work

Many previous papers from literature suggest analytic delay model[6][2] with fitting constants. However, if delay variability is as highly correlated to log-normal distributions as reported to be, a simple scheme of computing statistical extraction of mean(μ) and standard deviation(σ) with Monte Carlo simulation should be accurate enough, to some extent, enabling the validation of log-normal distribution. [3] uses a σ/μ model which has no dependence on input slew and output capacitance, and it is conventional for many other modeling work to neglect the effects of input slew and output capacitance or omit them from the results. Yet, Synopsys has recently brought LVF[5] into a standardized Liberty standard cell library format to account for the dependence of input slew and output capacitance. It makes sense that variability models should be validated throughout various slew/capacitance pairs.

3. Exploration Methodology

Our objective in this work is to validate the log-normal variability model with reference data obtained using Monte Carlo simulation in HSPICE. Spice simulation has been performed using a fab-provided 65nm BSIM4 model. All cells are designed using LVT transistors. Input slew and output capacitance has been adjusted to account for the variability of output slew. The analysis targets 92 timing arcs from 22 cells in total, each of which include 56 slew/capacitance conditions. We also have performed slew analysis as state-of-the-art OCV methodologies such as AOCV, POCV, LVF[4] consider both delay and slew as modeling targets of variability. Our target V_{dd} is 0.5V and target operating temperature is 25 °C

3.1 Determining Reference Value

In order to compare the variability estimates derived from variation distributions, reference values are required. We have performed a Monte Carlo analysis with 10,000 iterations in order to obtain the golden reference of 3 sigma delay values, although in most cases, analysis of 1,000 to 2,000 iterations is enough for variability characterization. The reference -3 sigma and +3 sigma delay value is each acquired by sorting the widely distributed 10,000 samples obtained with Monte Carlo analysis and selecting a value that lie at 3 standard deviation point, i.e. 99.73rd percentile from the highest and the lowest value, respectively.

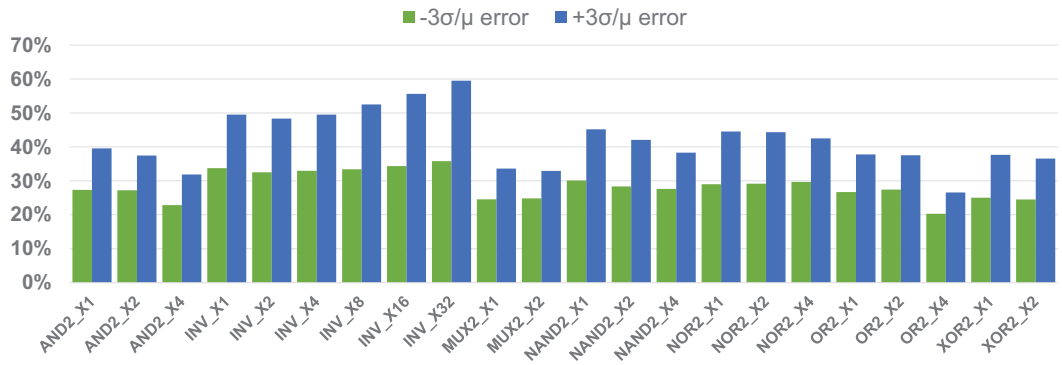

Figure 1. Average $\pm 3\sigma/\mu$ delay error by cell.

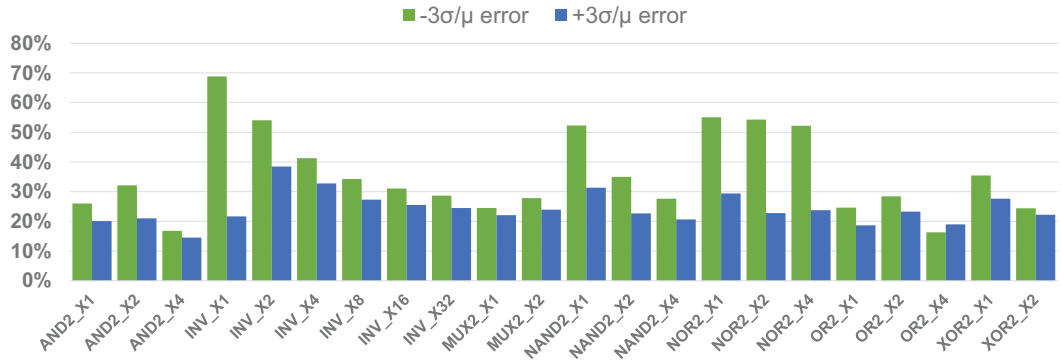

Figure 2. Average $\pm 3\sigma/\mu$ slew error by cell.

3.2 Modeling Methodology

We use the formulae introduced in [1], which compute mean(μ_{log}) and standard deviation(σ_{log}) of log(Td), where Td is delay of a gate cell from input to output, following normal distribution by definition. According to [1], 3σ worst case T_d can be computed by:

$$T_{d,3\sigma} = exp(\mu_{log} + 3\sigma_{log}) \tag{1}$$

where μ_{log} and σ_{log} can be computed by:

$$\mu_{log} = \ln\left(\frac{\mu^2}{\sqrt{\sigma^2+\mu^2}}\right) \tag{2}$$

$$\sigma_{log} = \sqrt{\ln\left(\frac{\sigma^2}{\mu^2}+1\right)}, \tag{3}$$

where μ and σ are mean and standard deviation calculated directly from the Monte Carlo iteration data, respectively. Our main interest in this work is to show how the real variability and its approximated model differ with different slew/capacitance condition, not the modeling method itself. Therefore we use (1) as our modeling methodology without any assumptions or approximations on parametric variation. We also omit any exploration on fitting methodology and only use statistical data to compute the log-normal distribution and find 3 σ error.

4. Results

Figure 1 and Figure 2 each depicts average $\pm 3\sigma/\mu$ delay and slew error, respectively. Average $+3\sigma/\mu$ and $-3\sigma/\mu$ delay error is each 49% and 27%, respectively, while $+3\sigma/\mu$ and $-3\sigma/\mu$ slew error is each 24% and 34%, respectively. Delay error seems consistent over a variety of cells Despite the ostensibly high error, real delay and slew variability error, i.e. $\mu + 3\sigma$ value, is each 28% and 11%, respectively. As for error dependency on slew and capacitance, we have averaged all cells by slew and capacitance in order to observe a macroscopic trend as depicted in Figure 3 and Figure 4. In the x-axis, the load capacitance is incremented first from 0.00005pF to 0.00906pF, and start over from 0.00005pF as slew is increased. Figure 3 shows an average delay error below 20% for most conditions with slew below 3ns, point at which the error starts to accumulate. This trend can be observed across most cells, while the trend of slew, as shown in Figure 4 show higher error rate at modest slew range. We can also note that the difference is less visible across load capacitance, depending more on input slew.

In order to look into the details of those higher error range and find out what cells occur high error rate in Figure 3 and Figure 4, in Figure 5 and Figure 6, we each fixed slew to 24.414 and 0.625, respectively and split slew/delay by cell. It is interesting to observe that the tendency of having relatively high error values, whether we are looking at ouput slew or output delay, are shared across a variation of cells.

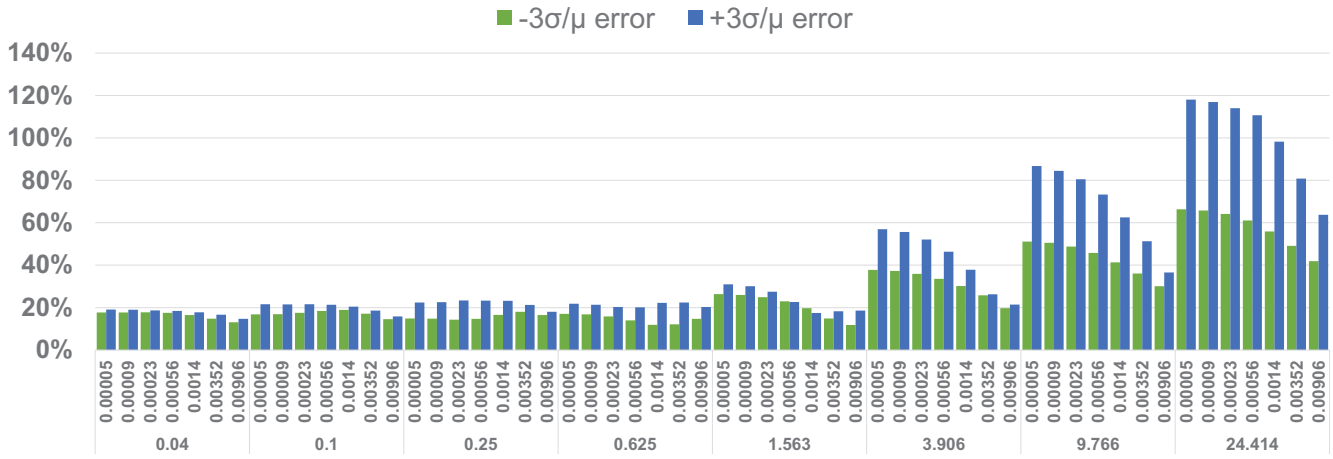

Figure 3. Average $\pm 3\sigma/\mu$ delay error of all cells. In x-axis, horizon figures indicate slew while vertical figures indicate capacitance. Error increases with lower output capacitance and higher input slew.

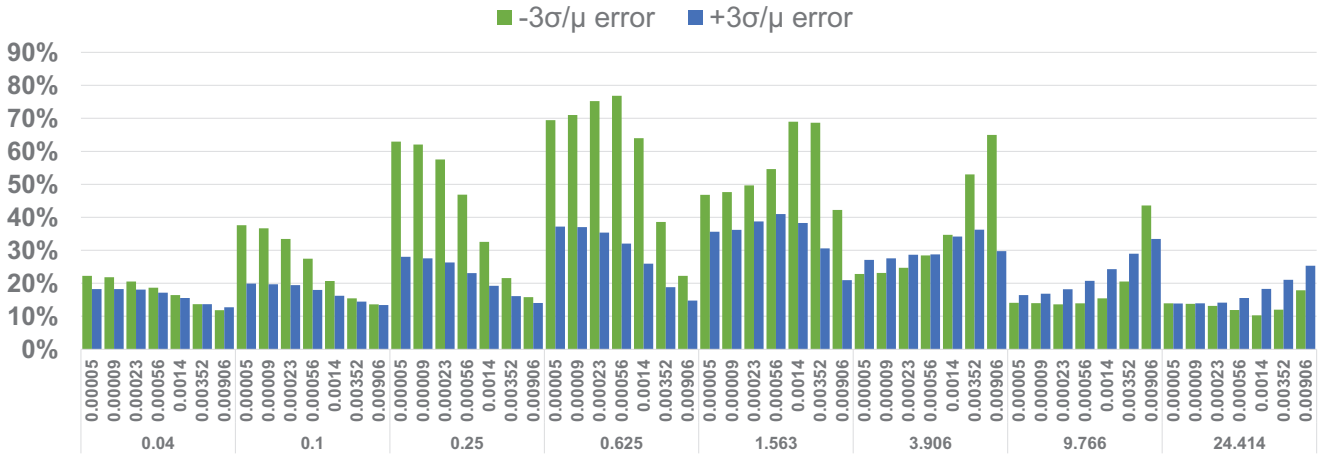

Figure 4. Average $\pm 3\sigma/\mu$ slew error of all cells. In x-axis, horizon figures indicate slew while vertical figures indicate capacitance. The observation made with delay error is not applicable here.

Meanwhile, It is worth mentioning that $\mu - 3\sigma$ error is highly overestimated due to its values approaching zero or simply negative. This effect causes the $\mu - 3\sigma$ delay error to average 323%, while slew error averages 19%. For that reason, it is more appropriate to set $\pm 3\sigma/\mu$ as an error metric owing to its independence of delay/slew value characteristics. This is the reason for showing $\pm 3\sigma/\mu$ instead of $\mu \pm 3\sigma$, which is the real value in which we are interested.

5. Conclusion

In this paper, we performed a wide exploration on variability of standard cells operating at near threshold region. Validated throughout 22 cells, 92 timing arcs, and 56 slew/capacitance pair,the log-normal distribution is an accurate modeling method being a simple method yielding a moderate delay/slew error. Meanwhile, although delay error is acceptable in low-slew area, delay error in high-slew area and slew error in some conditions are higher than expected. Our future work will include a novel modeling methodology to shade the error, as well as further explorations on various voltage and temperature conditions.

6. Acknowledgment

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References

[1] Slimani, M., F. Silveira, and P. Matherat, "variability modeling in near-threshold CMOS digital circuits." *Microelectronics Journal*, vol. 46, no 12, pp. 1313-1324, December 2015.

[2] Calhoun, Benton H., and Anantha Chandrakasan. "Characterizing and modeling minimum energy operation for subthreshold circuits." *IEEE Proceedings of the 2006 International Symposium on Low Power Electronics and Design(ISLPED)*, 2004.

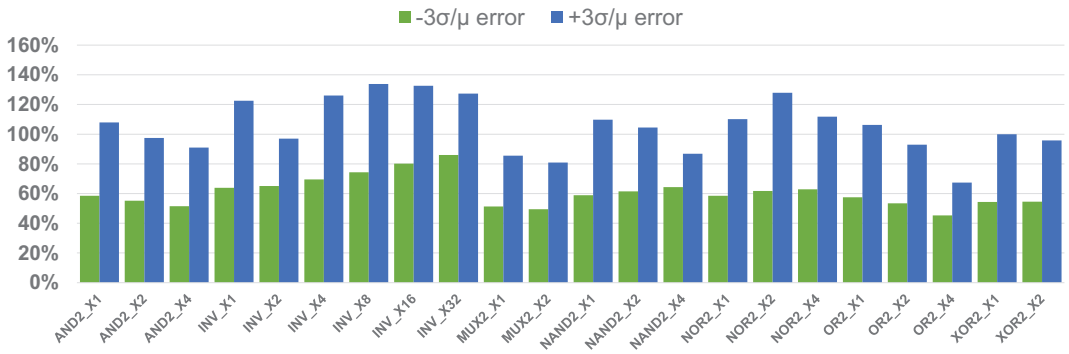

Figure 5. Average $\pm 3\sigma/\mu$ delay error by cell.

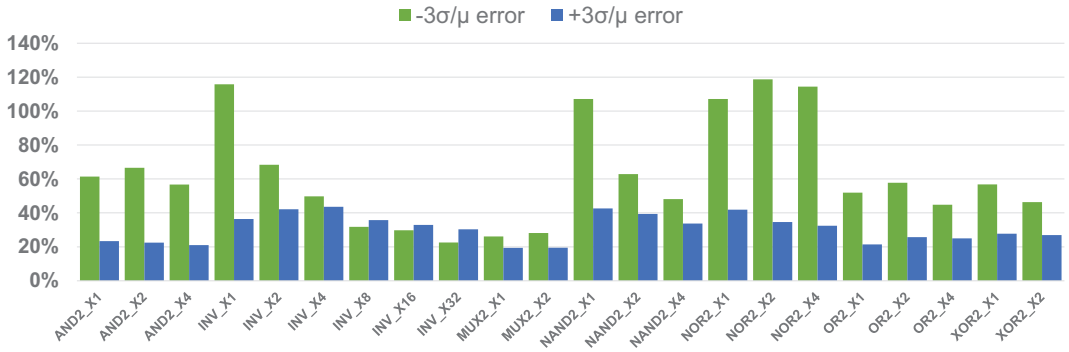

Figure 6. Average $\pm 3\sigma/\mu$ slew error by cell.

[3] Kwong, Joyce, and Anantha P. Chandrakasan. "Variation-driven device sizing for minimum energy sub-threshold circuits." *IEEE Proceedings of the 2006 International Symposium on Low Power Electronics and Design(ISLPED)*, 2006.

[4] SiliconSmart ACE User Guide, Version K-2016.06-SP2, Synopsys, December 2015.

[5] http://news.synopsys.com/2014-09-30-Synopsys-Announces-New-Additions-to-Liberty-to-Significantly-Speed-up-Timing-Closure

[6] Keller, Sean, David Money Harris, and Alain J. Martin. "A compact transregional model for digital CMOS circuits operating near threshold." *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* vol. 22 no. 10 pp. 2041-2053, September 2014.